

1/7

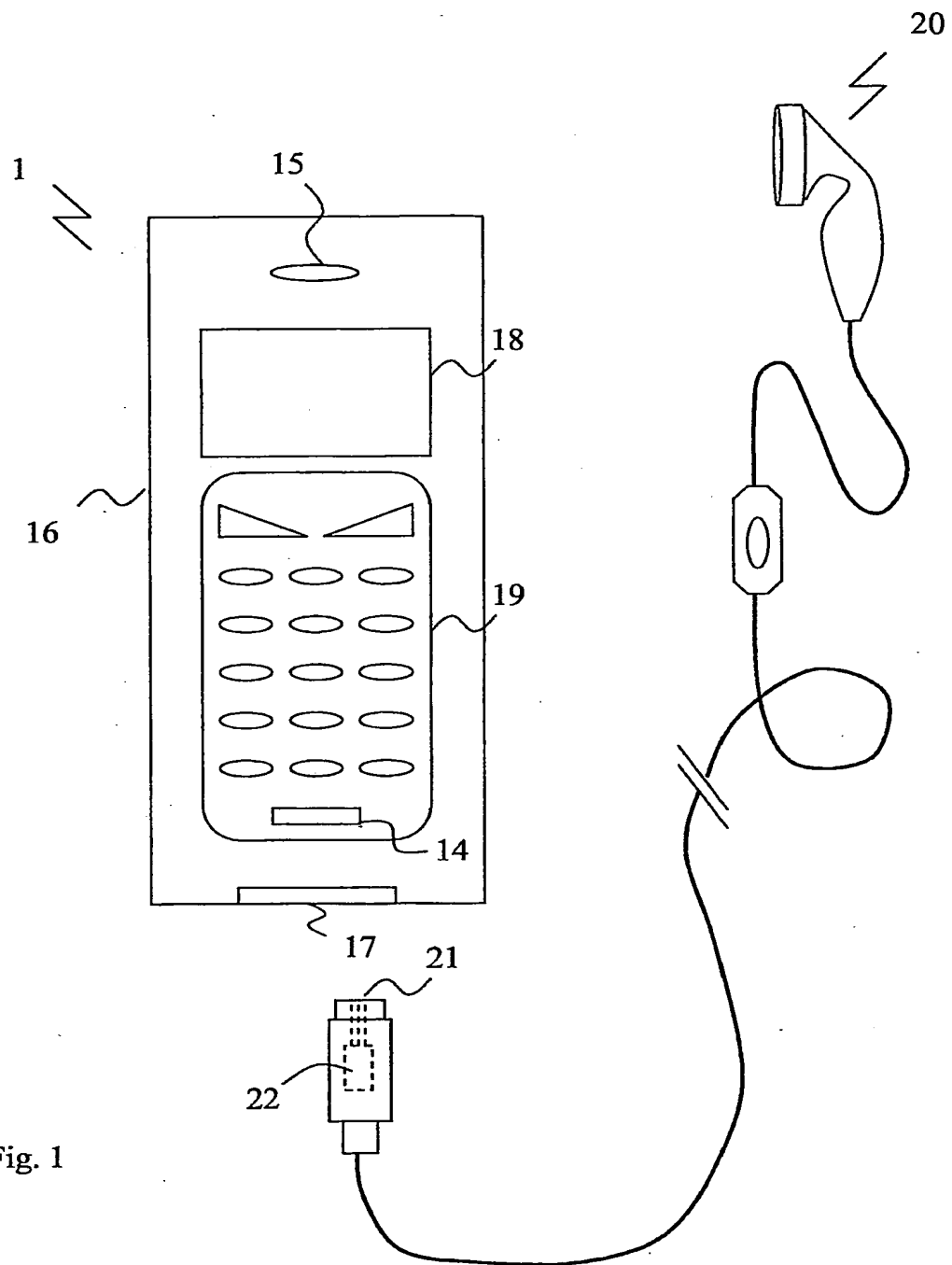


Fig. 1

2/7

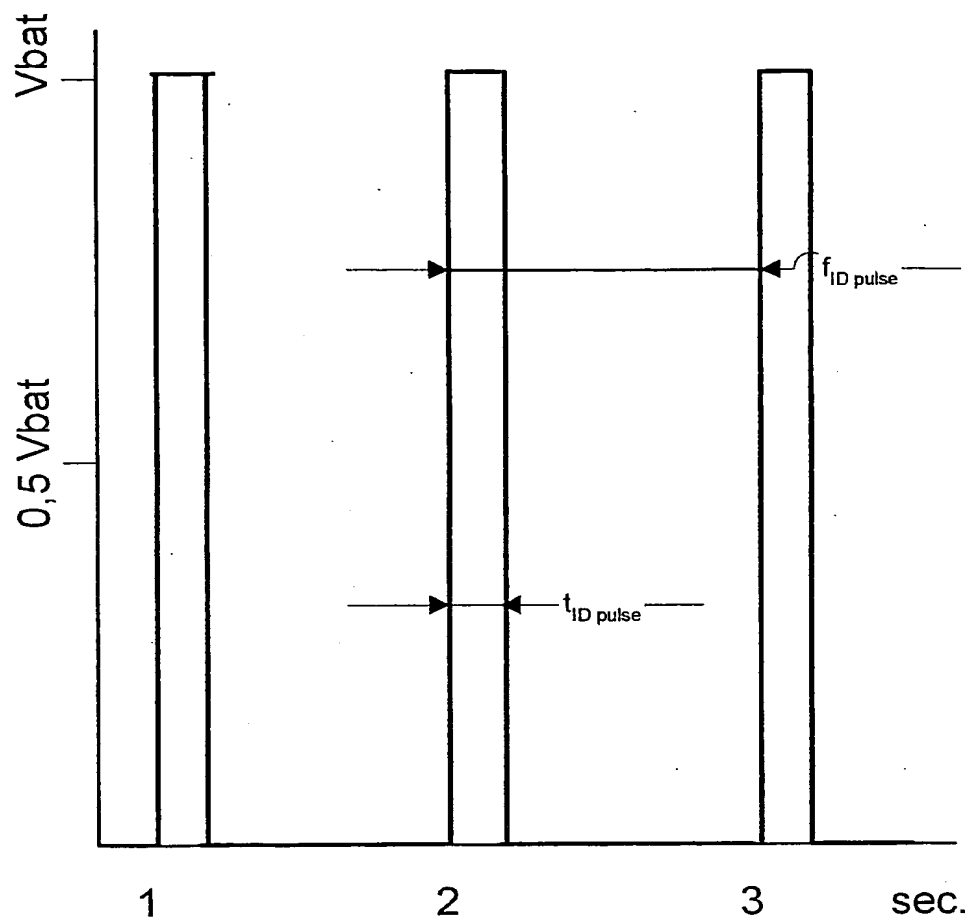


Fig. 2

3/7

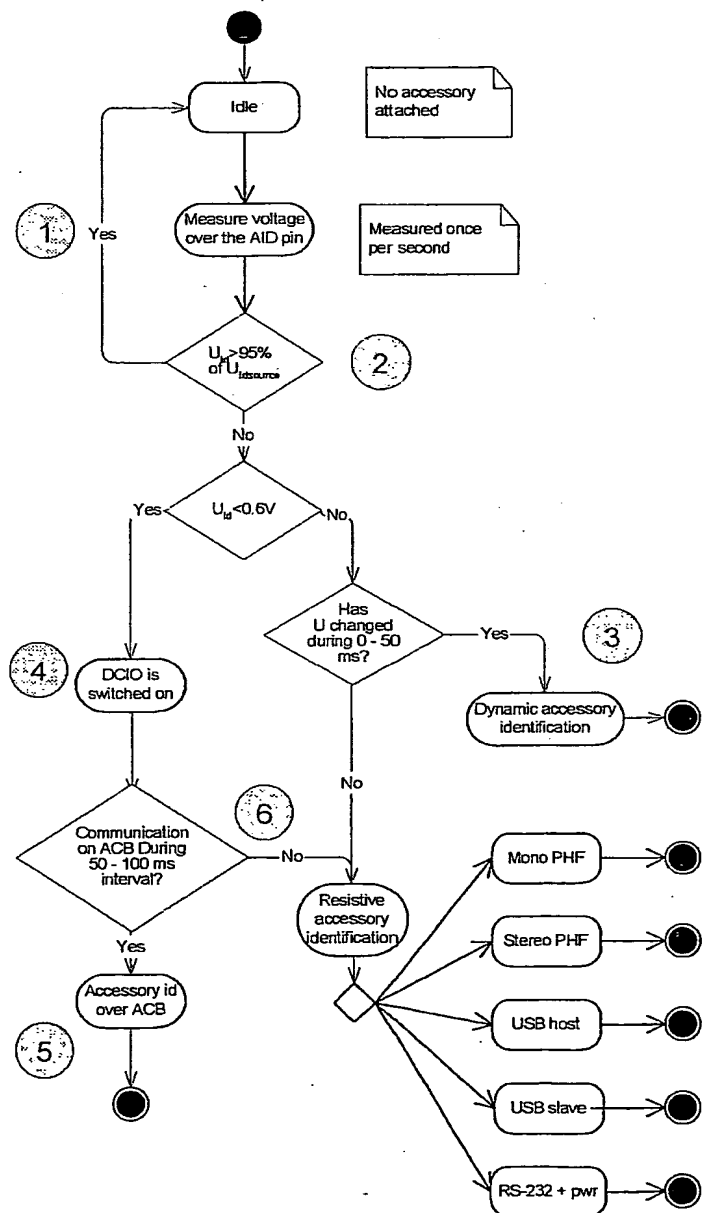


Fig. 3

4/7

## AID

Vdig [%]		Vdig [V]										First digit	
		0	1	2	3	4	5	6	7	8	9	0	1
100	2,75	F	F	F	F	F	F	F	F	F	F	F	F
95	2,61	E	E	E	E	E	E	E	E	E	E	E	E
90	2,48	D	D	D	D	D	D	D	D	D	D	D	D
85	2,34	C	C	C	C	C	C	C	C	C	C	C	C
80	2,20	B	B	B	B	B	B	B	B	B	B	B	B
75	2,06	A	A	A	A	A	A	A	A	A	A	A	A
70	1,93	0	0	0	0	0	0	0	0	0	0	0	0
65	1,79	9	9	9	9	9	9	9	9	9	9	9	9
60	1,65	8	8	8	8	8	8	8	8	8	8	8	8
55	1,51	7	7	7	7	7	7	7	7	7	7	7	7
50	1,38	6	6	6	6	6	6	6	6	6	6	6	6
45	1,24	5	5	5	5	5	5	5	5	5	5	5	5
40	1,10	4	4	4	4	4	4	4	4	4	4	4	4
35	0,96	3	3	3	3	3	3	3	3	3	3	3	3
30	0,83	2	2	2	2	2	2	2	2	2	2	2	2
25	0,69	1	1	1	1	1	1	1	1	1	1	1	1
20	0,55	Below AID electronics threshold voltage, usable for initiating Digital Accessory control bus.										5	5
15	0,41											4	4
10	0,28											3	3
5	0,14											2	2
0	0,00											1 (PFH)	1 (PFH)
												First digit = F	
												Resistor only lds	
												Digital signalling (if any) must start within this time-frame.	
												Second digit	
												time [s]	
												0,001	
												0,002	
												0,005	
												0,01	
												0,02	
												0,03 > 0,05 and < 0,1	
												∞	

Fig. 4

5/7

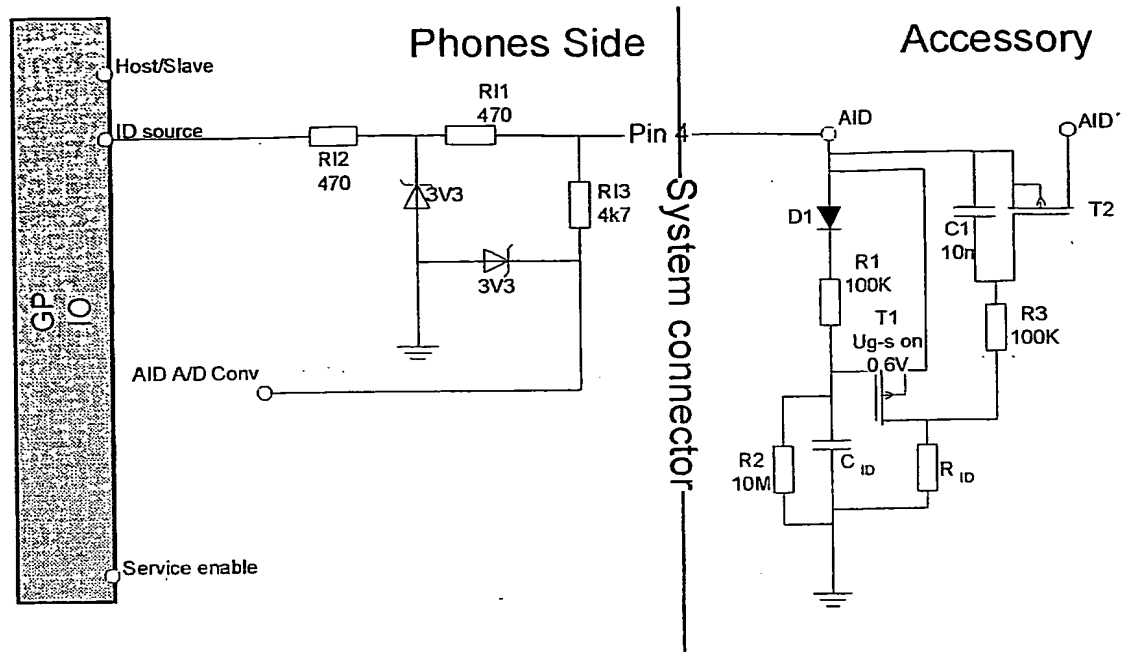


Fig. 5

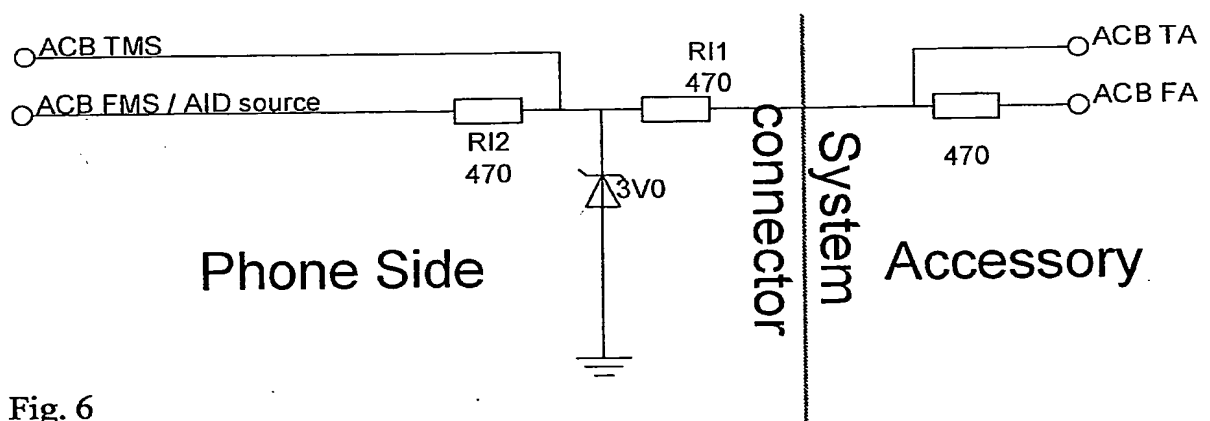


Fig. 6

6/7

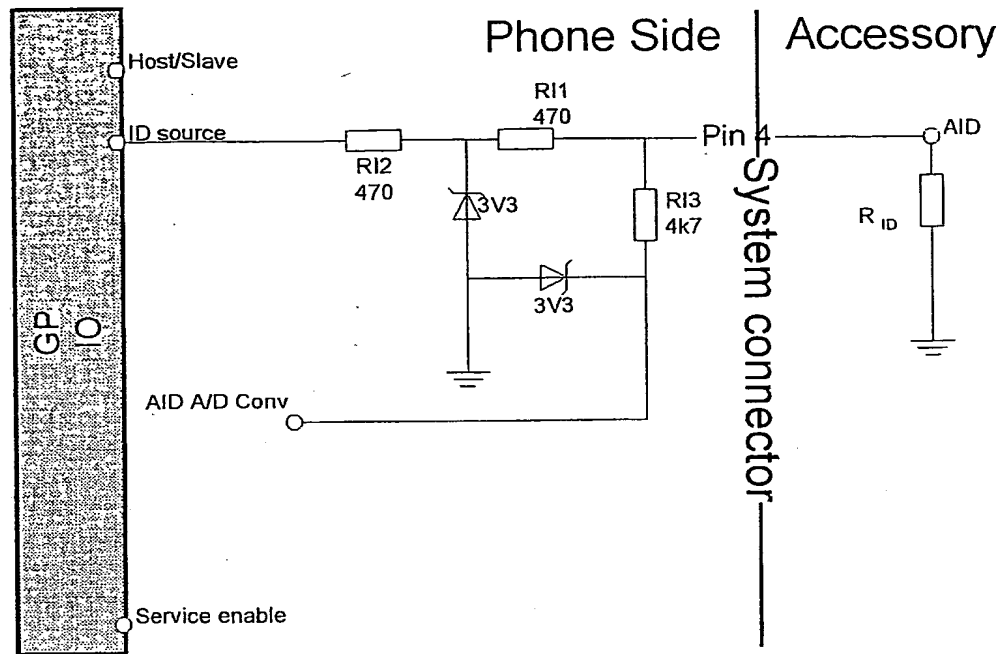


Fig. 7

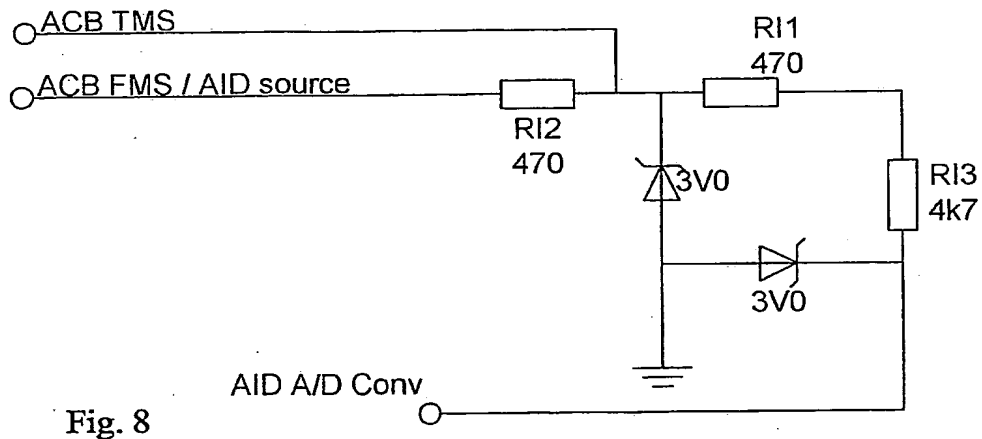


Fig. 8

717

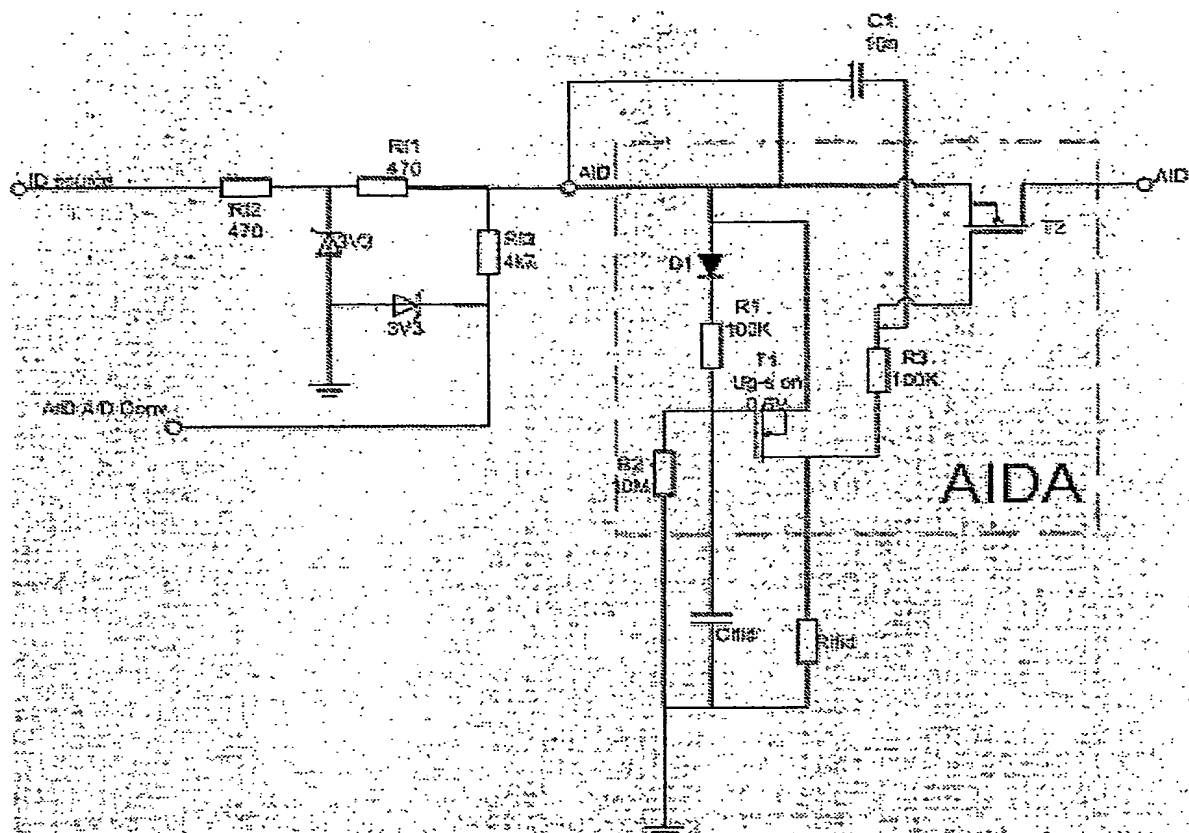


Fig. 9